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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,437	11/24/2003	Walter Anthony Wohlmuth	TRQ-00004	7134

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,437	WOHLMUTH, WALTER ANTHONY	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *18-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 03/27/2006, claims 1-27 are active in this application.

Claims 18-27 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected group there being no allowable generic or linking claim.

Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

Specification

2. The specification is objected to for the following reason: In the specification, page 3, line 16 (or paragraph [0007], line 2), the reference number "10" representing the substrate should be changed to –12-- in order to being consistent with what is/are shown in the drawing and described on line 3 of the same paragraph.

Claim Objection

3. The claim is objected to for the following reason: in claim 8, line 1, the word "substrate" should be changed to –structure-- in order to being in consistent with that defined in claim 7, line 3. Appropriate correction is required.

Remarks

4. Applicant's argument(s), filed 03/27/2006, with respect to claims 1-17 have been fully considered, but are moot in view of the new ground of rejections.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim(s) 1 is rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 5,243,207 to Plumton et al.

Regarding claim 1, Plumton discloses an integrated circuit comprising:

a depletion mode (D-mode) field effect transistor (FET) and an enhancement mode (E-mode) FET in a multi-layer structure (E/D-HFET, fig. 3),

wherein the multi-layer structure includes a semiconductor substrate 10 overlaid with a plurality of epitaxial semiconductor lavers 12, 14, 18, 20, 22 common to the D-

mode and E-mode FETS, including a channel layer 20/22 overlaid by a single barrier layer 26 overlaid by a first layer 28,

wherein the D-mode and E-mode FETS each include a source contact 48/42, a drain contact 52/46, and a gate contact 50/44, respectively, and

wherein the respective source and drain contacts 48/42 and 52/46 of the D-mode FET and E-mode FET are coupled to the first layer 28, and the respective gate contacts 50/44 of the D-mode FET and E-mode FET are coupled to the single barrier layer 26. See fig. 3.

Claim Rejections - 35 U.S.C. § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim(s) 2-6, 12, and 15-17 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 5,243,207 to Plumton et al., in view of U.S. Patent No. 6,452,221 to Lai et al.

Regarding claim 2, Plumton discloses the integrated circuit comprising all claimed limitations, including a Schottky contact (col. 4, lines 41-68). Plumton does not

expressly teach about a solid state amorphization region beneath the E-mode gate contact at least within the barrier layer.

Lai discloses a device, as shown in fig. 1, having a solid state amorphization region 40 beneath the E-mode gate contact 38 at least within the barrier layer 20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Plumton to have a solid state amorphization region be beneath the E-mode gate contact as that of Lai in order to provide excellent Schottky barrier to inhibit undesireable surface depletion effects in the adjacent regions between the recess edge and the gate metal. See col. 3, lines 18-27 of Lai.

Regarding claim 3, Plumton/Lai discloses the integrated circuit wherein the solid state amorphization region includes at least one compound including at least one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium. See col. 2, lines 55-65 of Lai.

Regarding claim 4, Plumton/Lai discloses the integrated circuit wherein the solid state amorphization region includes a plurality of compounds, wherein at least one of the compounds includes one of platinum, iridium, palladium, nickel, cobalt, chromium,

ruthenium, osmium, rodium, and rhenium, and at least one of the compounds includes a different one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium. See col. 2, lines 55-65 of Lai.

Regarding claim 5, Plumton/Lai discloses the integrated circuit wherein the multi-layer structure further comprises at least an epitaxial second layer (grading layer, col. 4, lines 1-4 of Plumton) between the barrier layer 26 and the first layer 28.

Regarding claim 6, Plumton/Lai discloses the integrated circuit wherein the barrier layer is of a first conductivity type; and further comprising an implant region of a second conductivity type formed at least in the barrier layer beneath the E-mode gate contact, wherein the solid state amorphization region is within the implant region. See fig. 1 and col. 2, lines 55-65 of Lai.

Regarding claim 12, Plumton discloses an integrated circuit (figs. 1-3) comprising:

a depletion mode (D-mode) field effect transistor (FET) and an enhancement mode (E-mode) FET (E/D-HFET, fig. 3) in a multi-layer structure,

wherein the multi-layer structure includes a semiconductor substrate 10 overlaid with a plurality of epitaxial semiconductor layers 12, 14, 18, 20, 22 common to the D-mode and E-mode FETS, including a channel layer 20/22 overlaid by a single barrier layer 26 overlaid at least by a first layer 28;

wherein the D-mode and E-mode FETS each include a source contact 48/42, a drain contact 52/46, and a gate contact 50/44, respectively,

wherein the source and drain contacts 48/52, and 42/46 of the D-mode FET and the E-mode FET, respectively, are coupled to one of the epitaxial layers 28 overlying the channel layer 20/22,

wherein a gate contact 50 of the D-mode FET is coupled to one of the first layer and the single barrier layer 26 (coupled to the barrier 26), and

wherein a gate contact 44 of the E-mode FET is coupled to one of the first layer and the single barrier layer 26 (coupled to the barrier 26).

Plumton also teaches about a Schottky contact (col. 4, lines 41-68); however, Plumton does not expressly teach about a solid state amorphization region beneath the E-mode gate contact at least within the barrier layer.

Lai discloses a device, as shown in fig. 1, having a solid state amorphization region 40 beneath the E-mode gate contact 38 at least within the barrier layer 20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Plumton to have a solid state amorphization region be beneath the D-mode and E-mode gate contacts as that of Lai in order to provide excellent Schottky barrier to inhibit undesireable surface depletion

effects in the adjacent regions between the recess edge and the gate metal. See col. 3, lines 18-27 of Lai.

Regarding claim 15, Plumton/Lai discloses the integrated circuit wherein the D-mode and E-mode source and drain contacts are coupled to the first layer 28, and the D-mode and E-mode gate contacts 50/44 are coupled to the barrier layer 26. See fig. 3 of Plumton.

Regarding claim 16, Plumton/Lai discloses the integrated circuit wherein the D-mode and E-mode source and drain contacts 48/52 and 42/46, respectively, are coupled to the first layer 28, and the E-mode gate contact 44 is coupled to the barrier layer 26. See fig. 3 of Plumton.

Regarding claim 17, Plumton/Lai discloses the integrated circuit wherein the barrier layer is of a first conductivity type; and further comprising an implant region of a second conductivity type formed at least in the barrier layer beneath the E-mode gate contact, wherein the E-mode solid state amorphization region is within the implant region. See fig. 1 and col. 2, lines 55-65 of Lai.

9. Claim(s) 7-13 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,078,067 to Oikawa., in view of U.S. Patent No. 6,452,221 to Lai et al.

Regarding claim 7, Oikawa discloses an integrated circuit, as shown in fig. 6, comprising:

a depletion mode field effect transistor (D-Type FET) and an enhancement mode (E-Type FET) in a multi-layer structure 101-109,

wherein the multi-layer structure includes a semiconductor substrate 101&102 overlaid with a plurality of epitaxial semiconductor layers 103-109 common to the D-mode and E-mode FETs, including a channel layer 103 overlaid by a single barrier layer 104 overlaid by a first layer 106 overlaid by a second layer (107-109) adjacent to the first layer 106,

wherein the D-mode and E-mode FETs each include a source contact 119/117, a drain contact 120/118, and a gate contact 116/115, respectively,

wherein the source and drain contacts 119/117 and 120/118 of the D-mode FET and the E-mode FET are coupled to the second layer (107-109), wherein the gate contact 116 of the D-mode FET is coupled to the first layer 106, and

wherein the gate contact 115 of the E-mode FET is coupled to the barrier layer 104.

Oikawa does not teach about a solid state amorphization region beneath the D-mode gate contact within the first layer and a solid state amorphization region beneath the E-mode gate contact within single the barrier layer.

Lai discloses a device, as shown in fig. 1, having a solid state amorphization region 40 beneath the gate contact 38 at least within the barrier layer 20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Oikawa to have a solid state amorphization region be beneath the D-mode and E-mode gate contacts as that of Lai in order to provide excellent Schottky barrier to inhibit undesireable surface depletion effects in the adjacent regions between the recess edge and the gate metal. See col. 3, lines 18-27 of Lai.

Regarding claim 8, Oikawa/Lai disclose the integrated circuit wherein the multi-layer structure includes an epitaxial third layer 105 between the first layer 106 and the barrier layer 104, said third layer 105 having a different composition than the first layer 106 and the barrier layer 14, and wherein the D-mode solid state amorphization region is within the third layer. See figs. 6, 8, and col. 7, line 50 to col. 8, line 38 of Oikawa, and fig. 1 of Lai.

Regarding claim 9, Oikawa/Lai discloses the integrated circuit wherein the barrier layer is of a first conductivity type; and further comprising an implant region of a second conductivity type formed at least in the barrier layer beneath the E-mode gate contact, wherein the E-mode solid state amorphization region is within the implant region. See figs. 6, 8 of Oikawa; and fig. 1 and col. 2, lines 55-65 of Lai.

Regarding claim 10, Oikawa/Lai discloses the integrated circuit wherein the D-mode and E-mode solid state amorphization regions include at least one compound including platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium. See col. 2, lines 55-65 of Lai.

Regarding claim 11, Plumton/Lai disclose the integrated circuit wherein the at least one of the D-mode and E-mode solid state amorphization regions includes a plurality of compounds, wherein at least one of the compounds includes one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium, rodium, and rhenium, and at least one of the compounds includes a different one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium, rodium, and rhenium. See col. 2, lines 55-65 of Lai.

Regarding claim 12, Oikawa discloses an integrated circuit (figs. 6, 8) comprising:

a depletion mode (D-mode) field effect transistor (D-Type FET) and an enhancement mode (E-Type FET) in a multi-layer structure 101-109,

wherein the multi-layer structure includes a semiconductor substrate 101&102 overlaid with a plurality of epitaxial semiconductor layers 103-109 common to the D-mode and E-mode FETS, including a channel layer 103 overlaid by a single barrier layer 104 overlaid at least by a first layer (106-109);

wherein the D-mode and E-mode FETS each include a source contact 119/117, a drain contact 120/118, and a gate contact 116/115, respectively,

wherein the source and drain contacts of the D-mode FET and the E-mode FET, are coupled to one of the epitaxial layers 104-109 overlying the channel layer 103,

wherein a gate contact 116 of the D-mode FET is coupled to one of the first layer and the single barrier layer (coupled to the first layer 106), and

wherein a gate contact 115 of the E-mode FET is coupled to one of the first layer and the single barrier layer (coupled to the barrier 104).

Oikawa does not expressly teach about a solid state amorphization region beneath the E-mode gate contact at least within the single barrier layer.

Lai discloses a device, as shown in fig. 1, having a solid state amorphization region 40 beneath the E-mode gate contact 38 at least within the barrier layer 20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Oikawa to have a solid state amorphization region be beneath the D-mode and E-mode gate contacts as that of Lai in order to provide excellent Schottky barrier to inhibit undesireable surface depletion effects in the adjacent regions between the recess edge and the gate metal. See col. 3, lines 18-27 of Lai.

Regarding claim 13, Oikawa/Lai discloses the integrated circuit wherein the D-mode gate contact 116 is coupled to the first layer 106, and the E-mode gate contact 115 is coupled to the barrier layer 104. See figs. 6, 8 of Oikawa.

Regarding claim 14, Oikawa/Lai discloses the integrated circuit further comprising a second solid state amorphization region disposed beneath the D-mode gate contact at least within the first layer. See the rejection of claim 7.

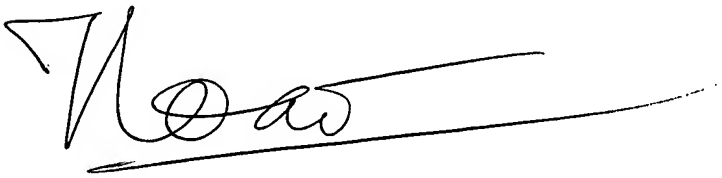
Conclusion

10. **THIS ACTION IS MADE FINAL.** A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao Nguyen whose telephone number is (571)272-

1791. The examiner can normally be reached on Monday-Friday 9:00am - 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571)272-1907. The fax numbers for all communication(s) is (571)273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.



ANDY HUYNH
PRIMARY EXAMINER

Dao H. Nguyen
Art Unit 2818
June 3, 2006